Tracking performance optimization of CMOS Monolithic Active Pixel Sensors

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Abstract

CMOS Monolithic Active Pixel Sensors (MAPS) provide an attractive solution for high precision tracking of minimum ionizing particles. A thin, moderately doped, undepleted silicon layer is used in these devices as a detector active volume with the readout electronics implemented on top of it. A new MAPS prototype has been fabricated using recently available AMS 0.35 µm OPTO process, featuring wafers with a 20 µm thick epitaxial layer. A systematic study of tracking performance of that prototype using high-energy particles beam is presented in this work. Detection efficiency, noise generated hit suppression and spatial resolution versus impact angle are shown as a function of readout pitch and charge collecting diode size. Two-particle tracks resolution calculated measured charge distributions is also discussed. A test array with a novel readout circuitry is included in the design. The circuit consists of a front-end voltage amplifier, with a gain of 5 or 10, capacitively coupled to the charge collecting diode and followed by two analog memory cells. This architecture implements an on-pixel correlated double sampling method, allowing for optimization of integration independently of full frame readout time and strongly reducing pixel-to-pixel output signal dispersion. Requirements for the precision of the data transmission and digitization are thus reduced in this solution Noise performance and output signal characteristics of that structure are measured and compared with a standard, two- or three-transistor solution.

Summary

A Monolithic Active Pixel Sensor (MAPS) integrates on the same substrate the detector element with the processing electronics and is fabricated using standard CMOS process available through many commercial microelectronics companies. The idea of using MAPS for the detection of ionizing radiation, in particular for high-energy charged particles tracking, has been proposed by the IReS-LEPSI team in the beginning of 1999. The ability of the monolithic CMOS sensors to provide charged particle tracking has been demonstrated on a series of MIMOSA (standing for Minimum Ionizing MOS Active sensor) chip prototypes [1-5]. The key element is the use of an N_well/P_substrate diode to collect through thermal diffusion the charge generated by the impinging particle in the thin, undepleted silicon layer underneath the readout electronics. This solution allows 100% fill factor, as required in tracking applications. It has been verified that both epitaxial and uniform-high resistivity (~10 Ω cm) substrates may be used for device fabrication [6]. The observed excellent tracking performance makes CMOS MAPS an interesting candidate for vertex detectors in future Particle Physics experiments and for ionizing radiation imaging in different applications. In order to optimize tracking performance as a function of pixel granularity, a new prototype Mimosa9 has been fabricated using recently available AMS 0.35 µm OPTO process. Providing high quality, 20-µm thick epitaxial layer on top of low resistivity substrate and very low N_well diode dark current, this process is perfectly matched for the application. The Mimosa9 prototype (Fig.1) contains four arrays of pixels with a pitch varying from 20 µm to 40 µm. Simple readout architecture is used (Fig.2). It consists of a 3-transistor pixel cell (one reference array) or a self-biased 2-transistor cell (three arrays dedicated for particle tracking). Charge collecting diodes of different sizes are used for each readout pitch, in order to optimize the signal-to-noise ratio and spatial resolution. A systematic study of tracking performances of all structures using high-energy particles beam is presented in this work. Detection efficiency, noise generated hit suppression and spatial resolution for different impact angles are shown as a function of the readout pitch and the diode geometry. Two-particle hit resolution calculated using measured charge distributions is also discussed. The same pixel structures are available also on a high-resistivity wafer; therefore, a direct comparison of epitaxial and non-epitaxial substrate is possible. Fig.3 shows the resolution measured with the array having 40 µm readout pitch and non-epitaxial substrate type (the worst case example).

A structure with a novel readout circuitry is also included in the design. It consists of the front-end voltage amplifier, with a gain of 5 or 10, capacitively coupled to the charge collecting diode and followed by two analog memory cells (Fig.4). This architecture implements an on-pixel correlated double sampling method, allowing for optimization of integration independently of full frame readout time and strongly reducing pixel-to-pixel output signal dispersion. Requirements for the precision of the data transmission and digitization are released in this solution, which is of importance for a higher readout clock frequency. Several versions of this amplifier are tested. The basic one (Fig.5) allows a voltage gain of five, applying a simple cascode structure. An integrated capacitive coupling between the charge-collecting element and the amplifier is essential for an independent and optimal biasing (through V_{bias} and V_{inp}) of the N_well diode and of the cascode. The amplifier version with a higher gain (x10) uses thicker gate oxide transistors available in that fabrication process. The layout of this simple circuit fits easily a 30 µm pixel size (Fig.6), with storage capacitors values allowing precise signal sampling. The proposed solution is a candidate for STAR microvertex upgrade, to be operated at room temperature with a very simple airflow cooling system and high data throughput (in the order of one million samples per trigger) on a single transmission line. Availability of the full analog information at the external acquisition board, related to this solution, will allow a flexible digital filtering of unexpected electromagnetic perturbation (common mode pick-up), providing an additional safety factor. Noise performance and output signal characteristics of that structure are measured and compared with a standard, two- or three-transistor solution.

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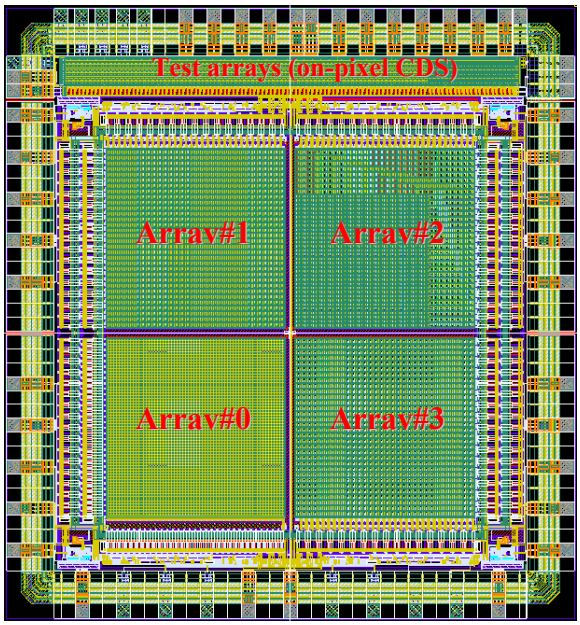

Fig.1

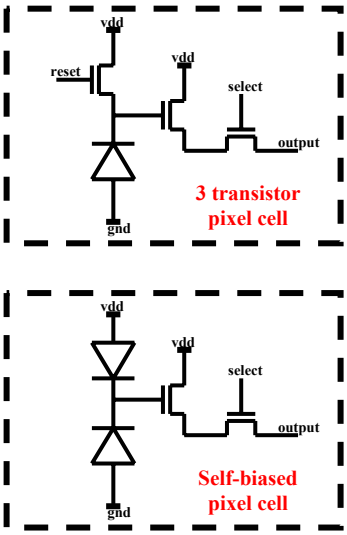

Fig.2

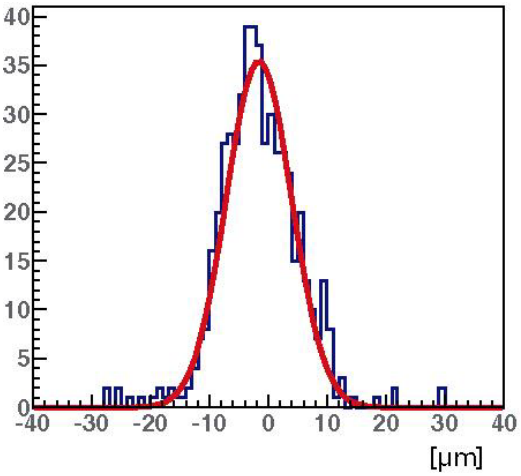

Fig.3

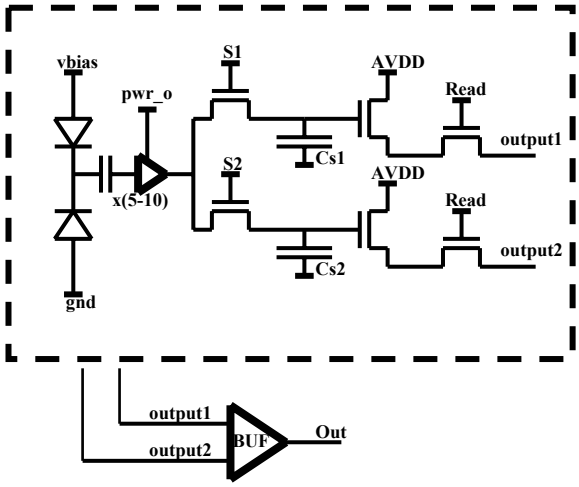

Fig.4

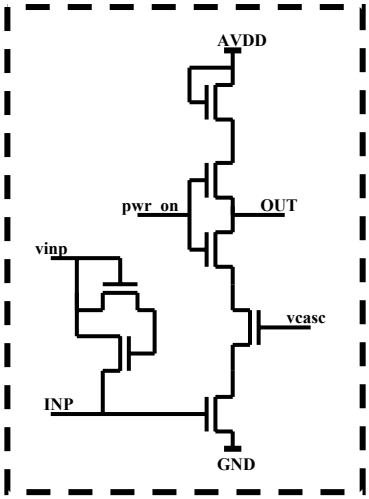

Fig.5

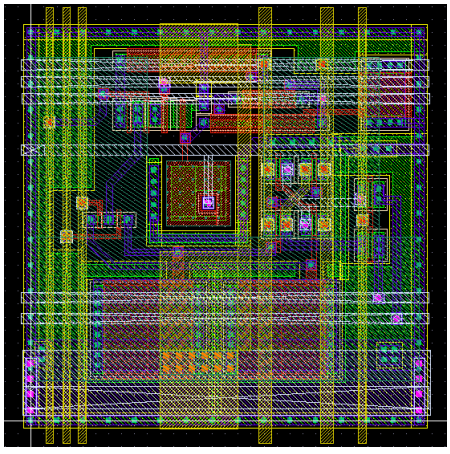

Fig.6